A 65 nm Logic Technology Featuring 35 nm Gate Length, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57um^2 SRAM Cell

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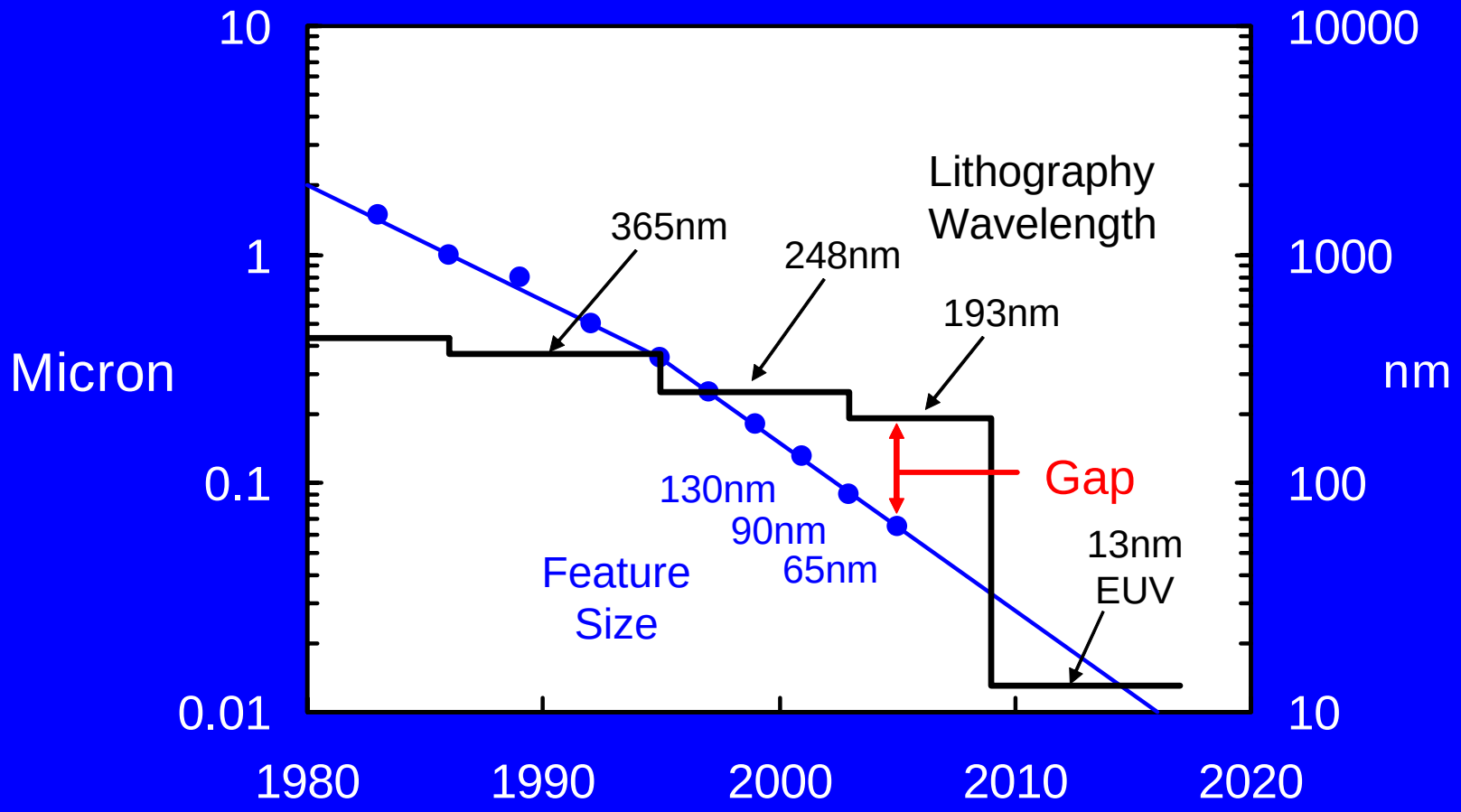
Outline

- 65 nm technology dimensional scaling
- Transistor features and performance
- Interconnect features and performance
- SRAM test vehicle
- Conclusion

Lithography Challenge at 65 nm

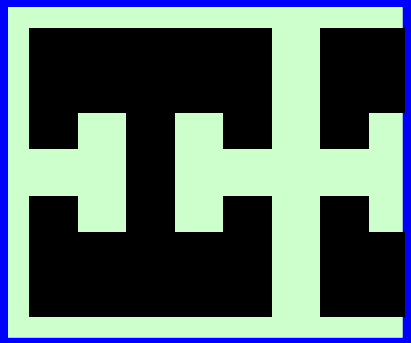


Minimum feature size at significant gap to lithography wavelength

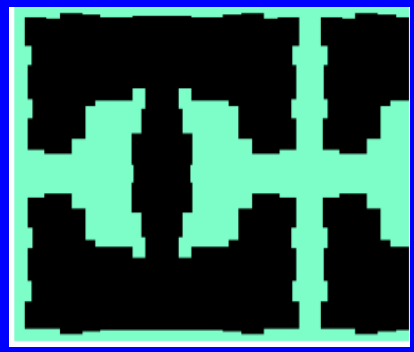
Advanced photomask techniques help to bridge the gap

Leading-Edge OPC and APSM Masks

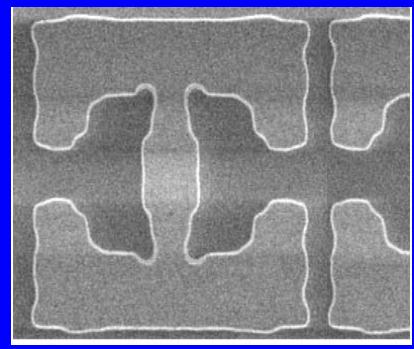
Sub-resolution Optical Proximity Correction



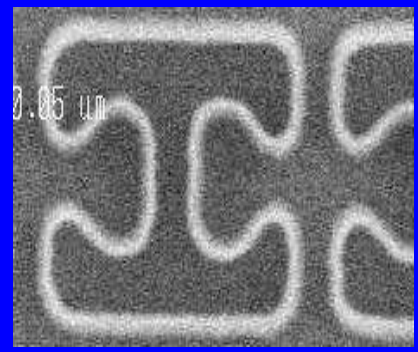
Drawn structure



Add OPC features

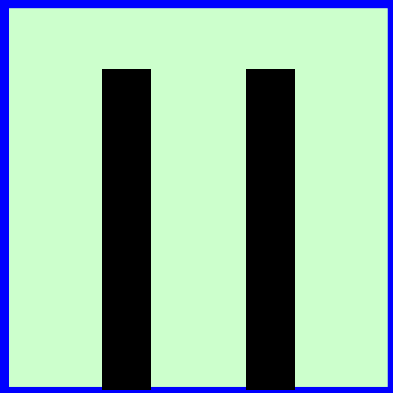


Mask structure

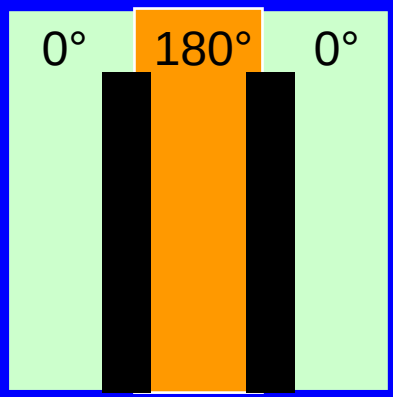


Printed on wafer

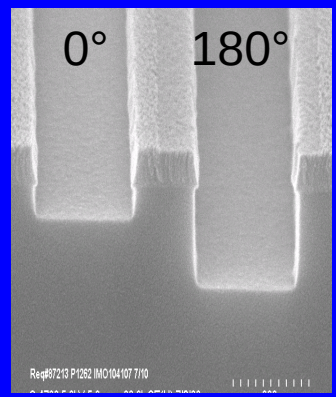
Phase shift masks enable patterning 35 nm lines



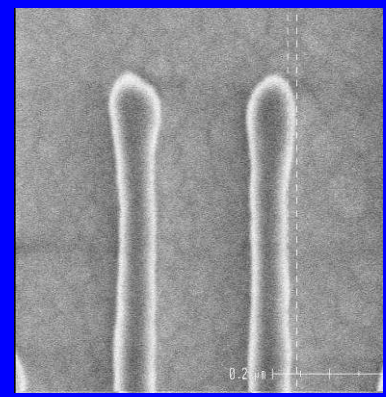
Drawn structure



Add phase regions



Mask structure



Printed on wafer

Aggressive Design Rule and Metal AR

Layer	Pitch (nm)	Thickness (nm)	Aspect Ratio
Isolation	220	320	NA
Poly silicon	220	90	NA
Contacted gate	220	NA	NA
Metal 1	210	170	1.6
Metal 2	210	190	1.8
Metal 3	220	200	1.8
Metal 4	280	250	1.8
Metal 5	330	300	1.8
Metal 6	480	430	1.8
Metal 7	720	650	1.8
Metal 8	1080	975	1.8

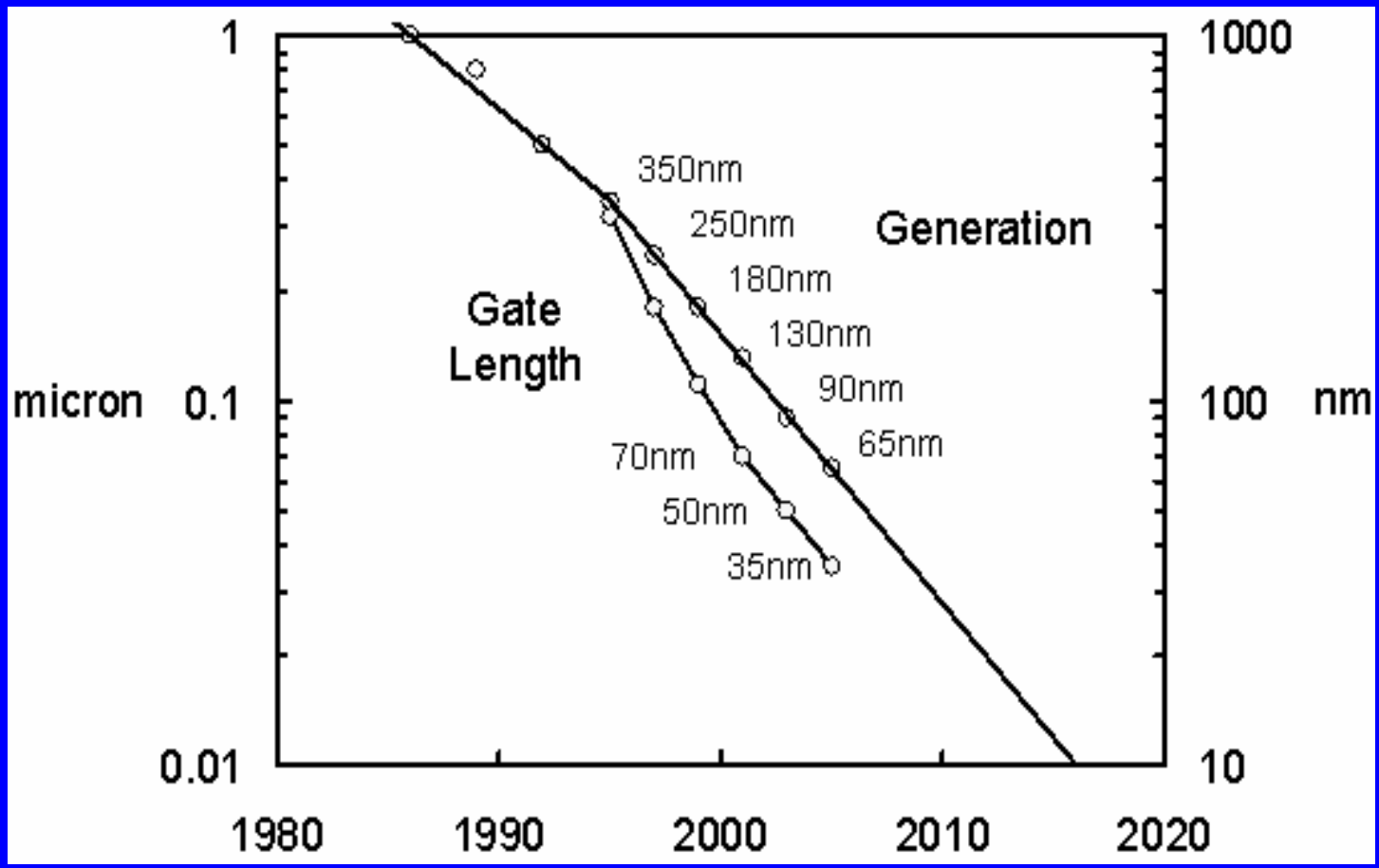
65 nm node continues ~70% linear scaling

Metal aspect ratio optimized for RC delay

Transistor Features

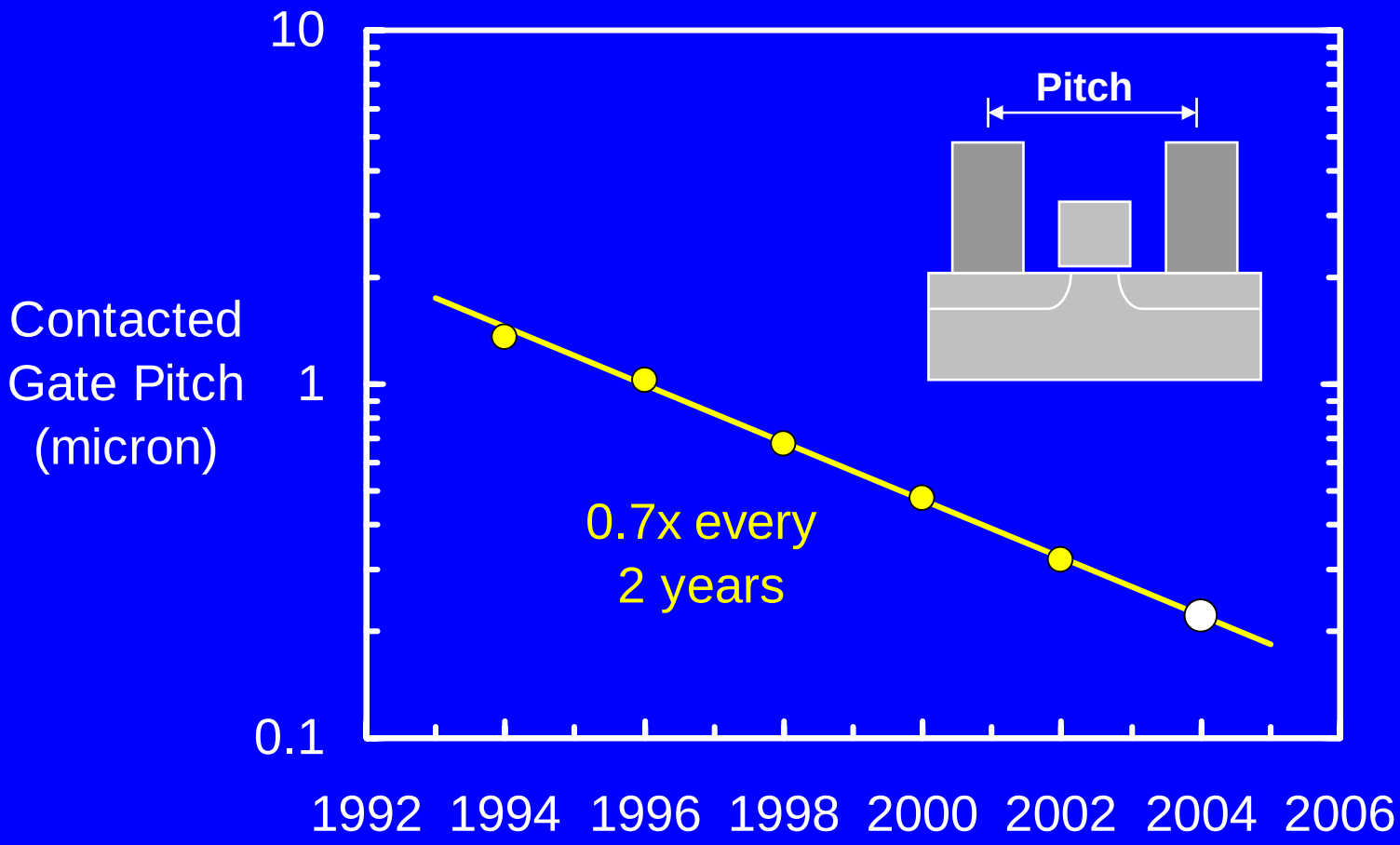
- 35 nm gate length
- 220 nm contacted gate pitch
- 1.2 nm physical gate oxide
- 2ND generation of strained silicon
- NiSi salicide

Logic Transistor Gate Length Trend



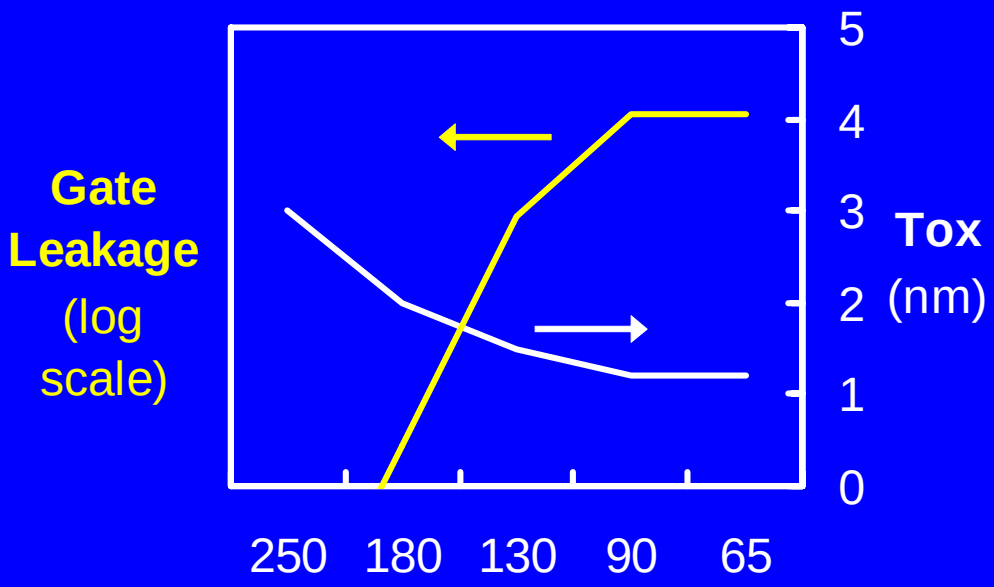
65 nm continues aggressive gate length scaling

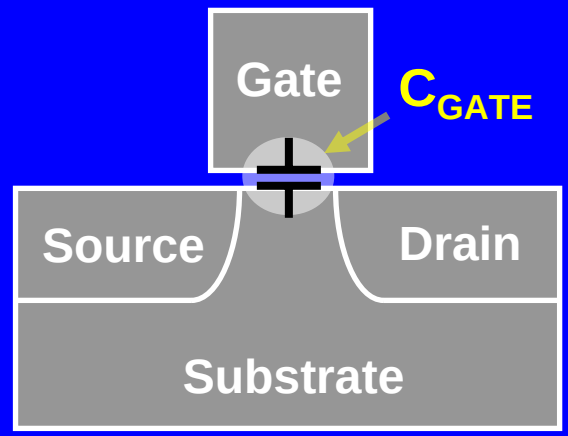
Contacted Gate Pitch



Transistor gate pitch continues to scale 0.7x per generation, now 220 nm on 65 nm generation

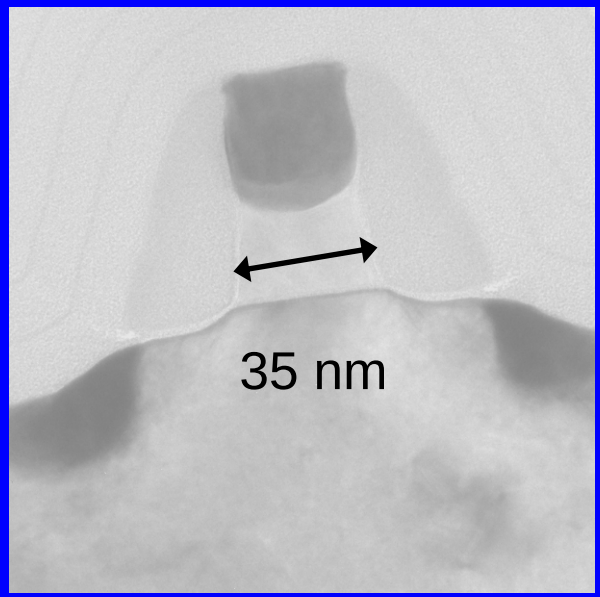
1.2 nm Gate Oxide

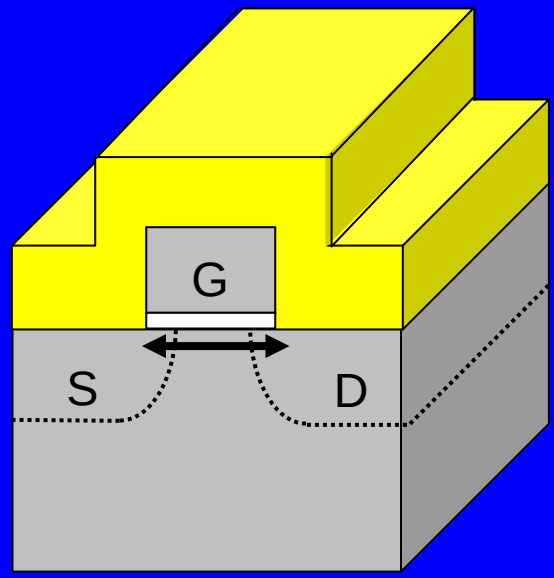




- **Gate oxide thickness is held at 1.2 nm to avoid increased gate leakage**
- **Gate capacitance (C_{GATE}) reduced ~20% due to smaller gate length (35 nm)**
- **Lower gate capacitance improves performance and reduces active power**

NMOS with Enhanced Strain

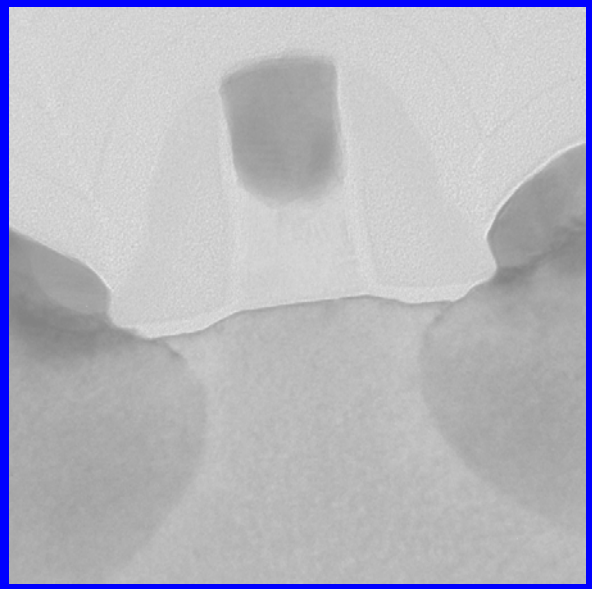


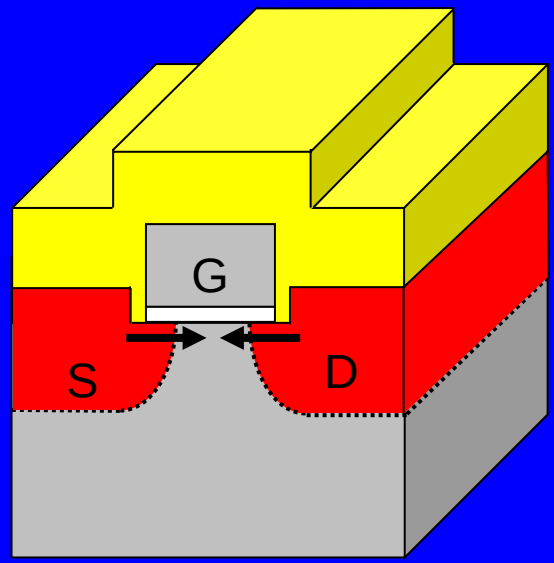


Tensile SiN capping films for enhanced uniaxial strain

Shallow/abrupt junction for SCE control for 35 nm gate

PMOS with Enhanced Strain





Epitaxial SiGe film embedded into S/D – same as 90 nm

Enhanced strain by higher Ge content in SiGe film

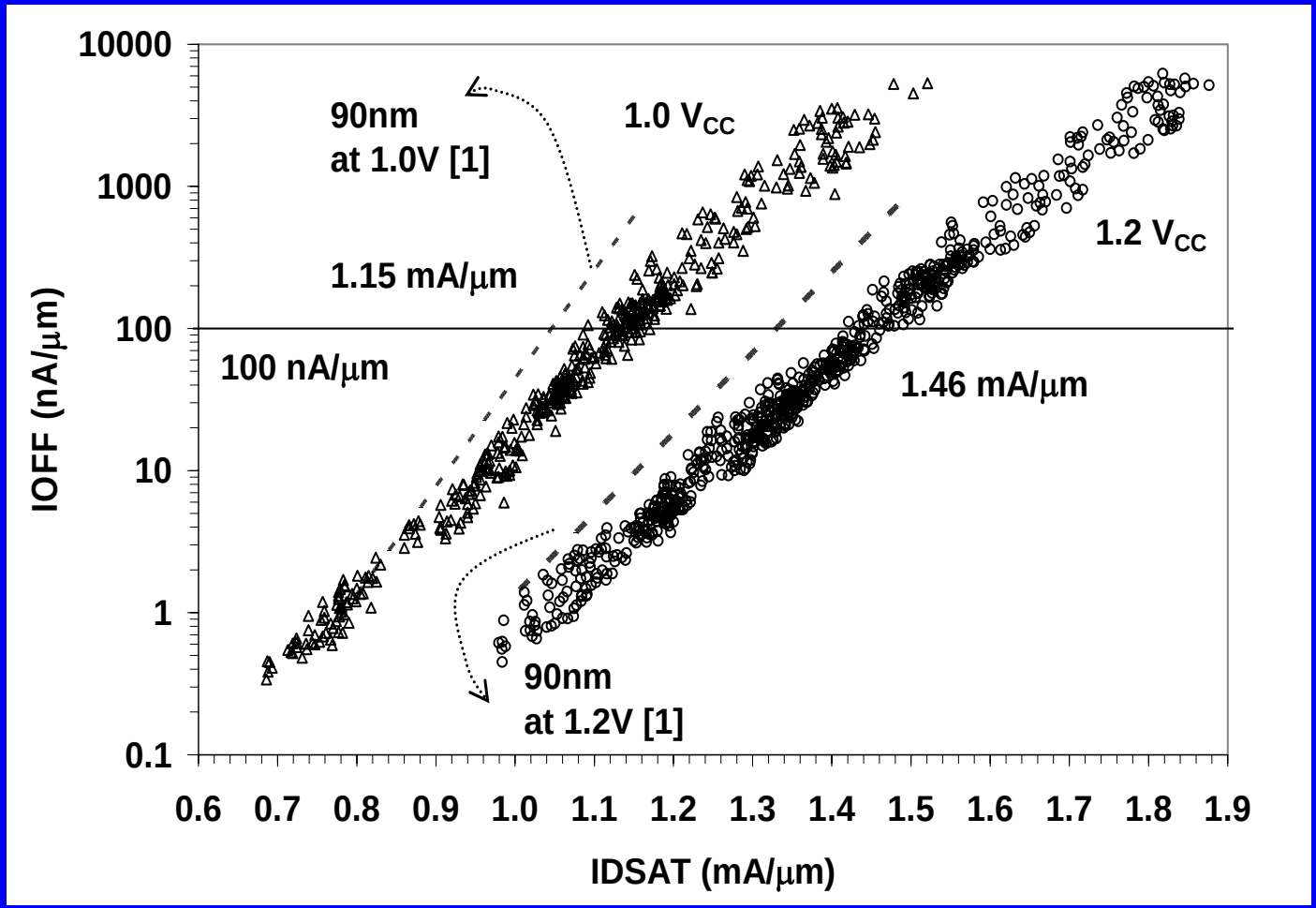
Intel 2ND Generation Strained Silicon

Strain-induced performance gain summary

	90 nm		65 nm	
	NMOS	PMOS	NMOS	PMOS
Mobility	20%	55%	35%	90%
I_{DSAT}	10%	30%	18%	50%
I_{DLIN}	10%	55%	18%	80%

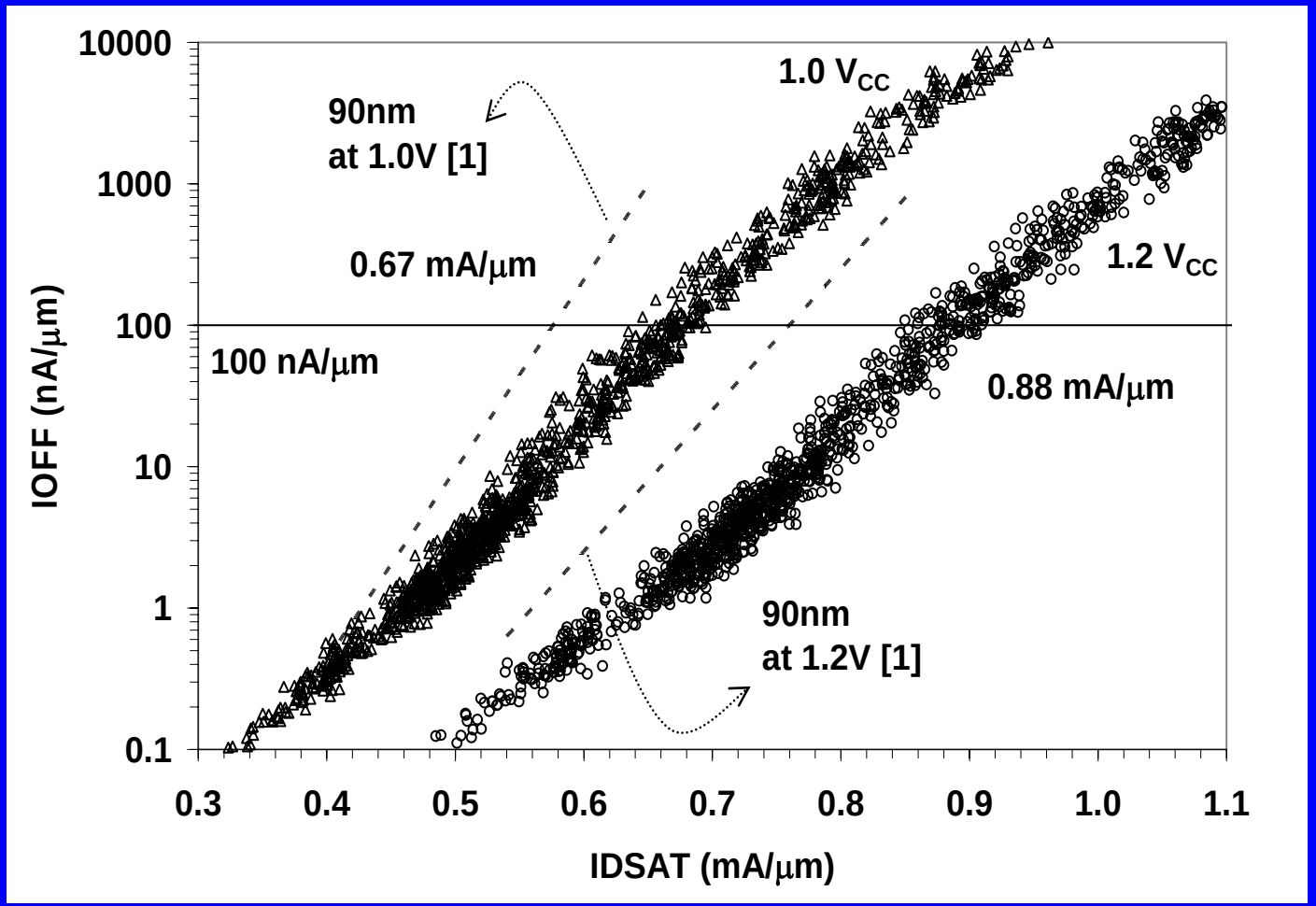
65 nm transistors improve strain over 90 nm

NMOS I_{DSAT} vs I_{OFF}



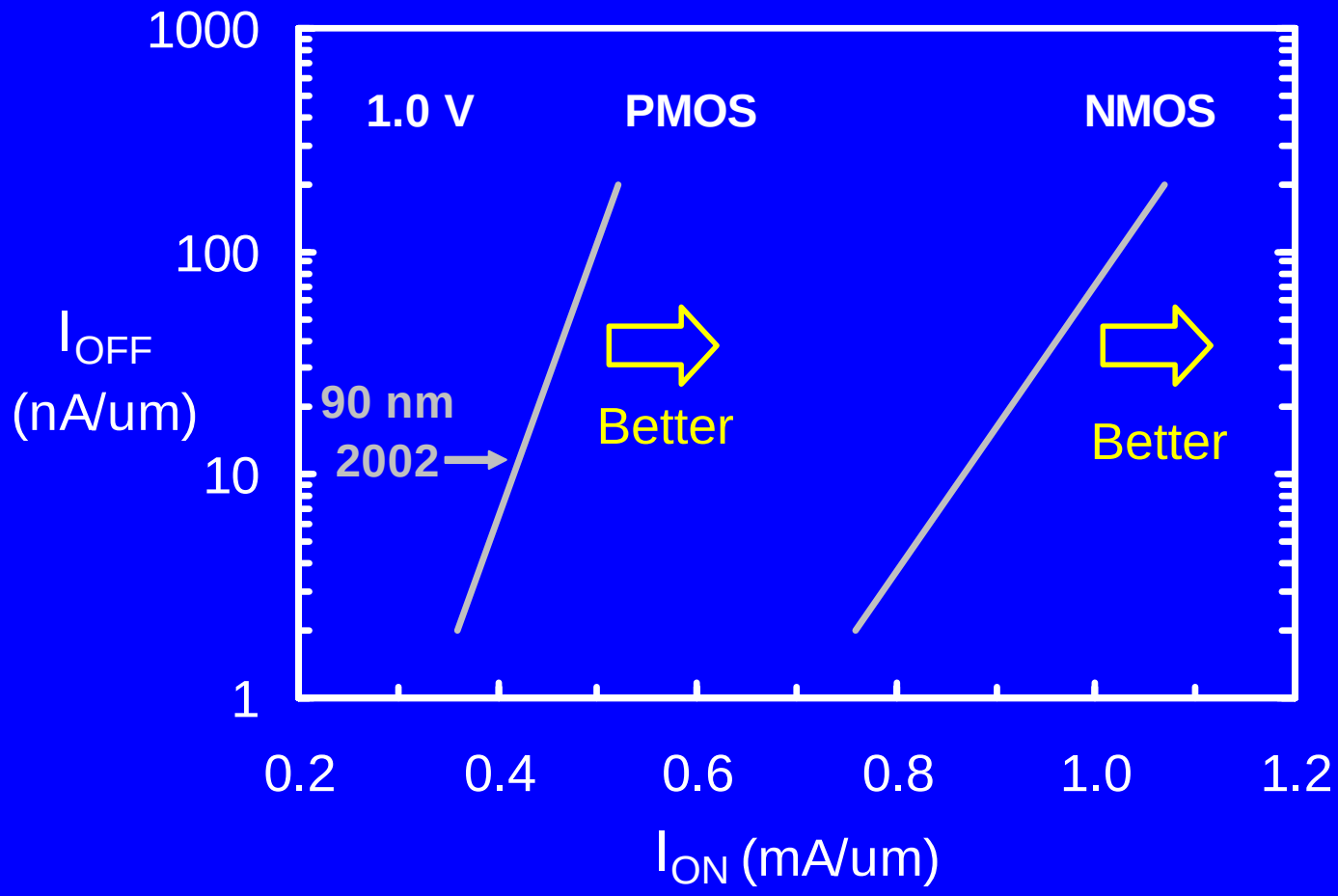
Record 1.46 mA/μm I_{DSAT} at 1.2 V and 100 nA/μm I_{OFF}

PMOS I_{DSAT} vs I_{OFF}



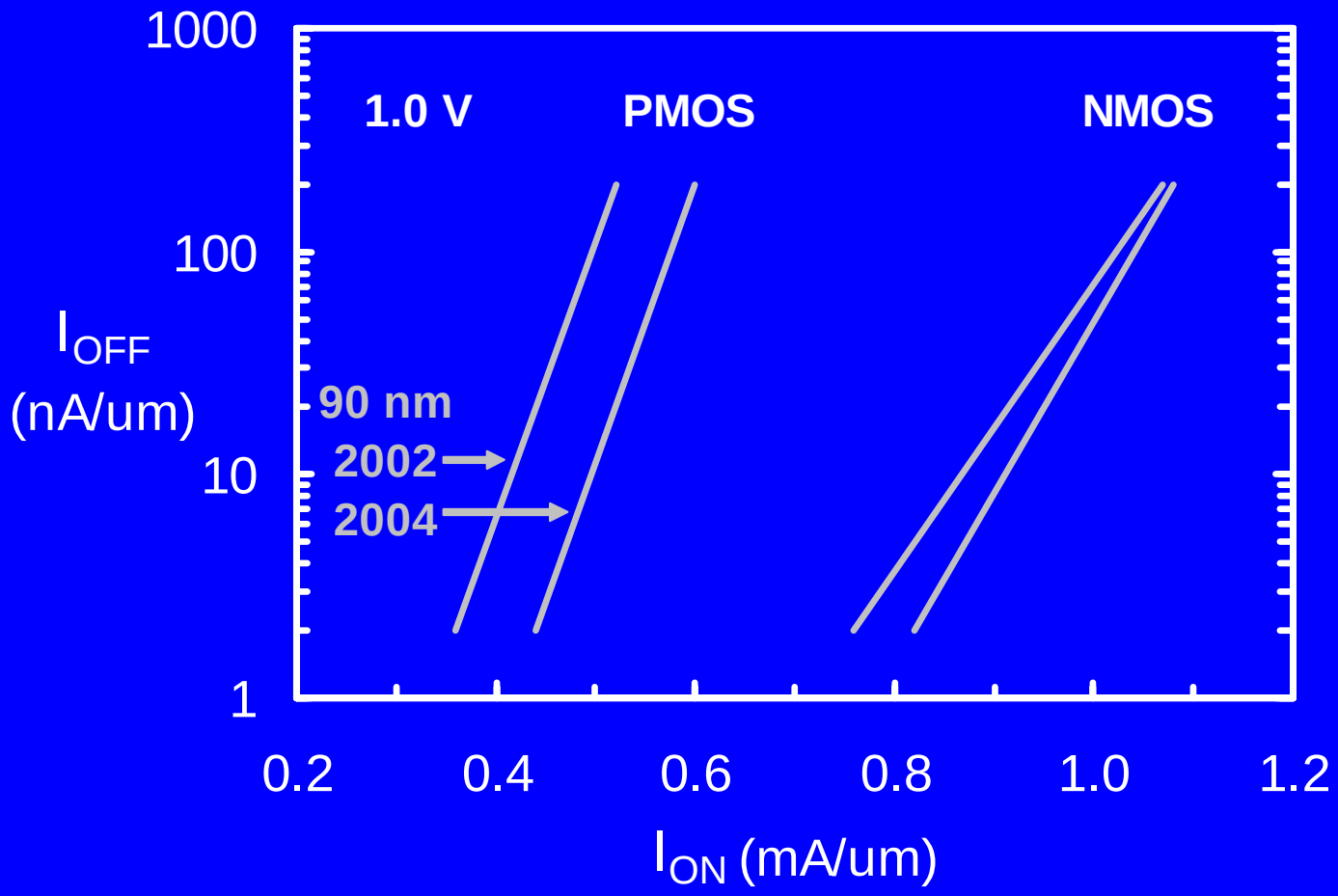
Record 0.88 mA/μm I_{DSAT} at 1.2 V and 100 nA/μm I_{OFF}

Improved Transistor Performance



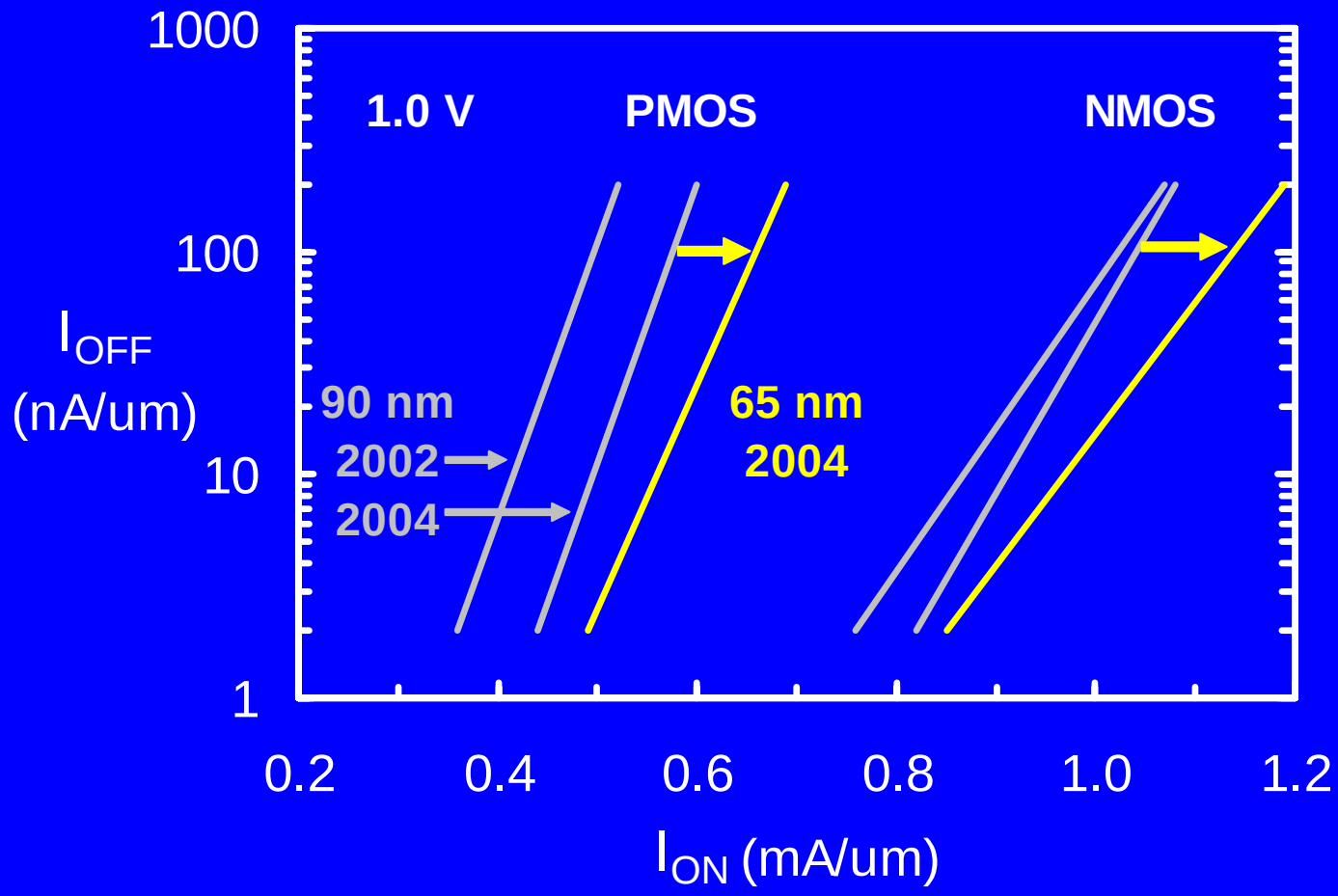
Improved transistors provide increased drive current at constant leakage current

Improved Transistor Performance



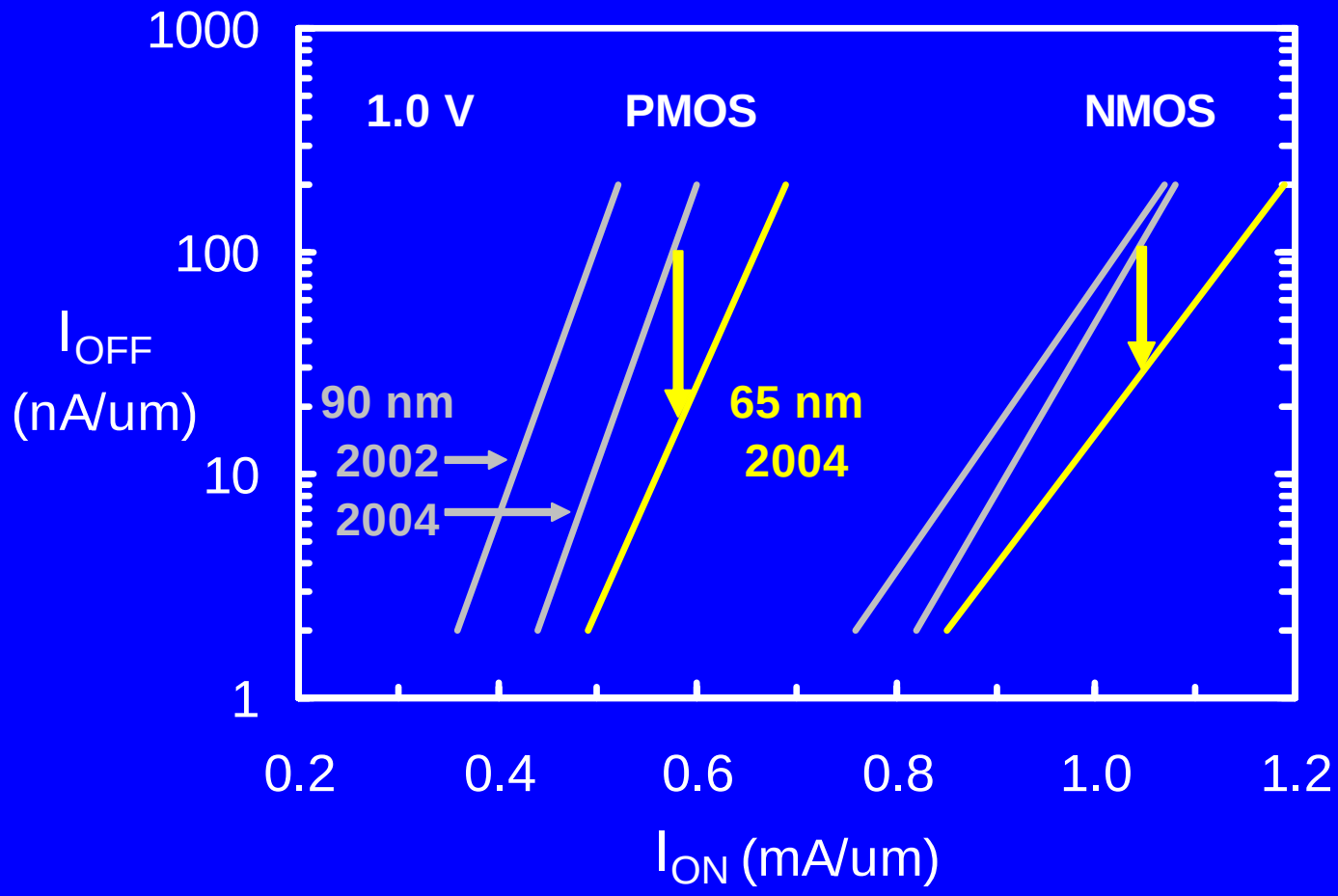
90 nm transistors have continued to improve

Improved Transistor Performance



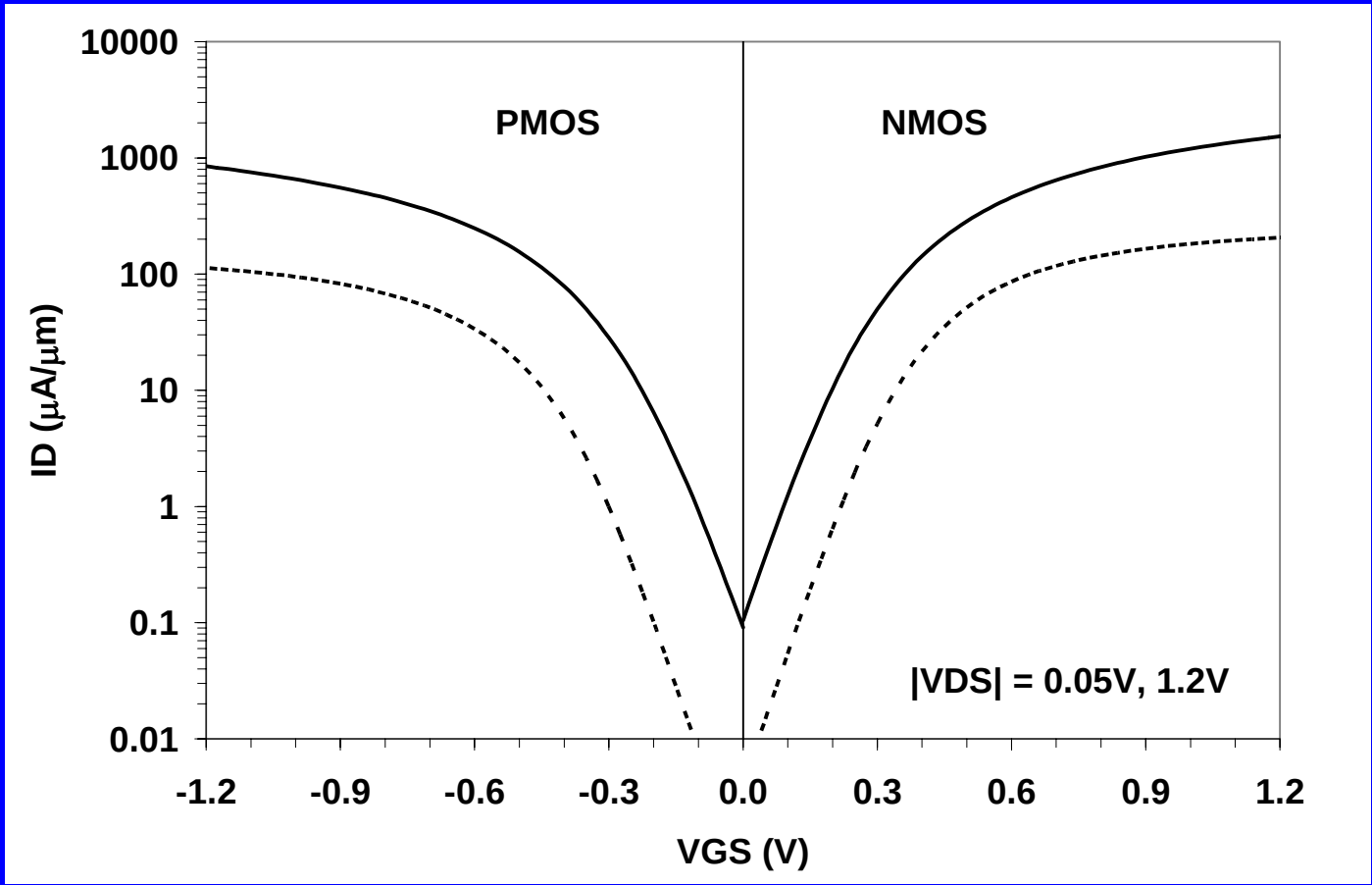
65 nm transistors increase drive current 10-15% with enhanced strain

Improved Transistor Performance



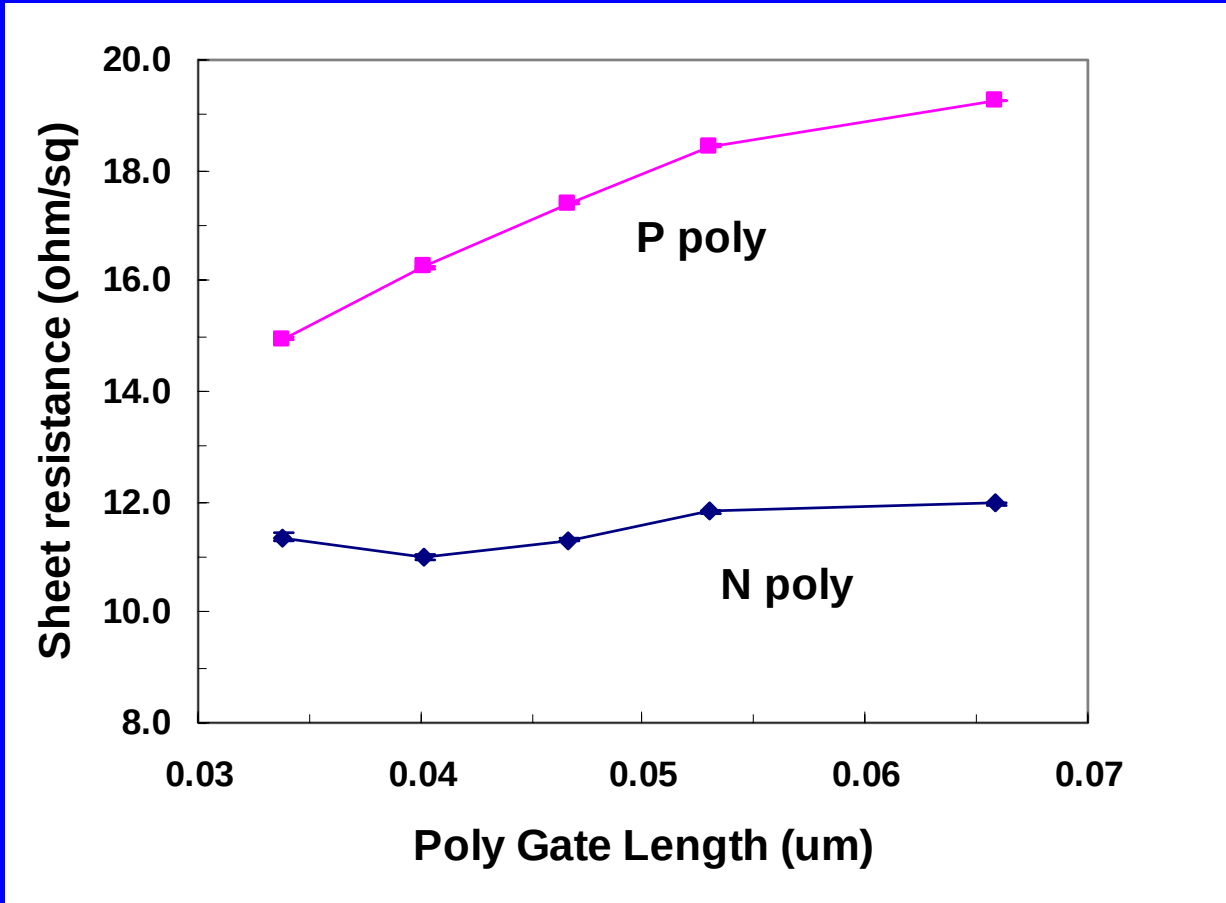
65 nm transistors can alternatively provide ~4x leakage reduction

Sub-threshold Characteristics



Well controlled short channel effects
Sub-threshold slope ~100 mV/decade

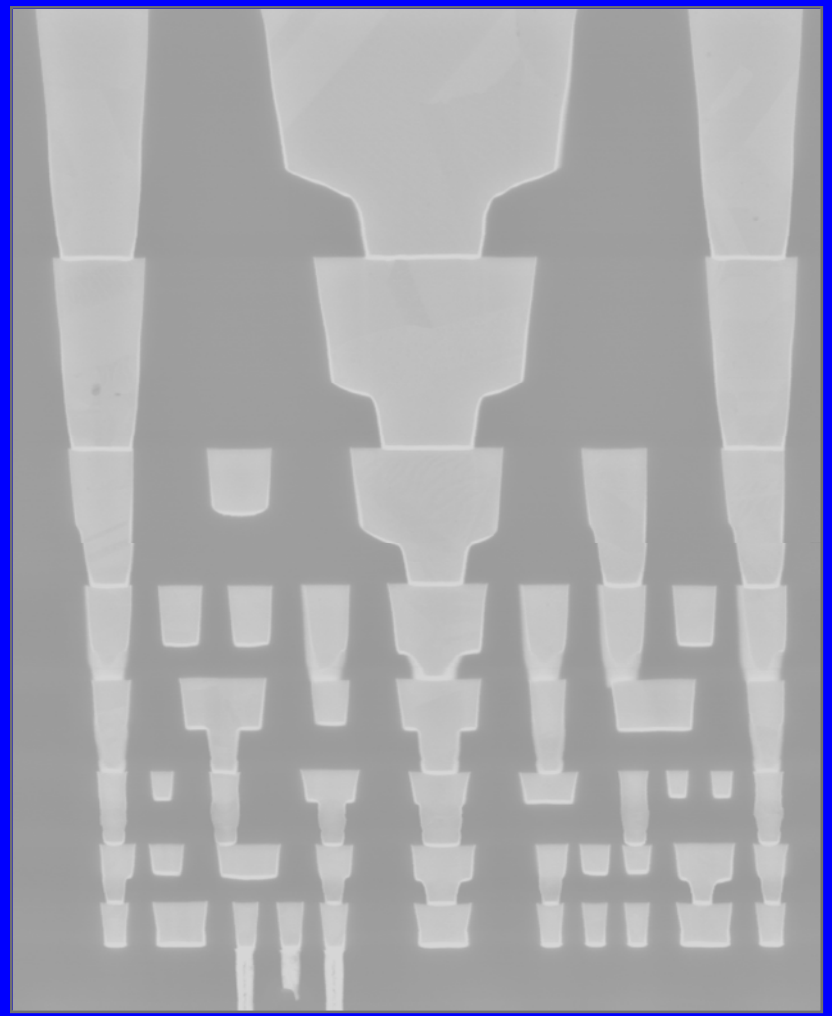
Ni Salicide Capable for 35 nm Gate



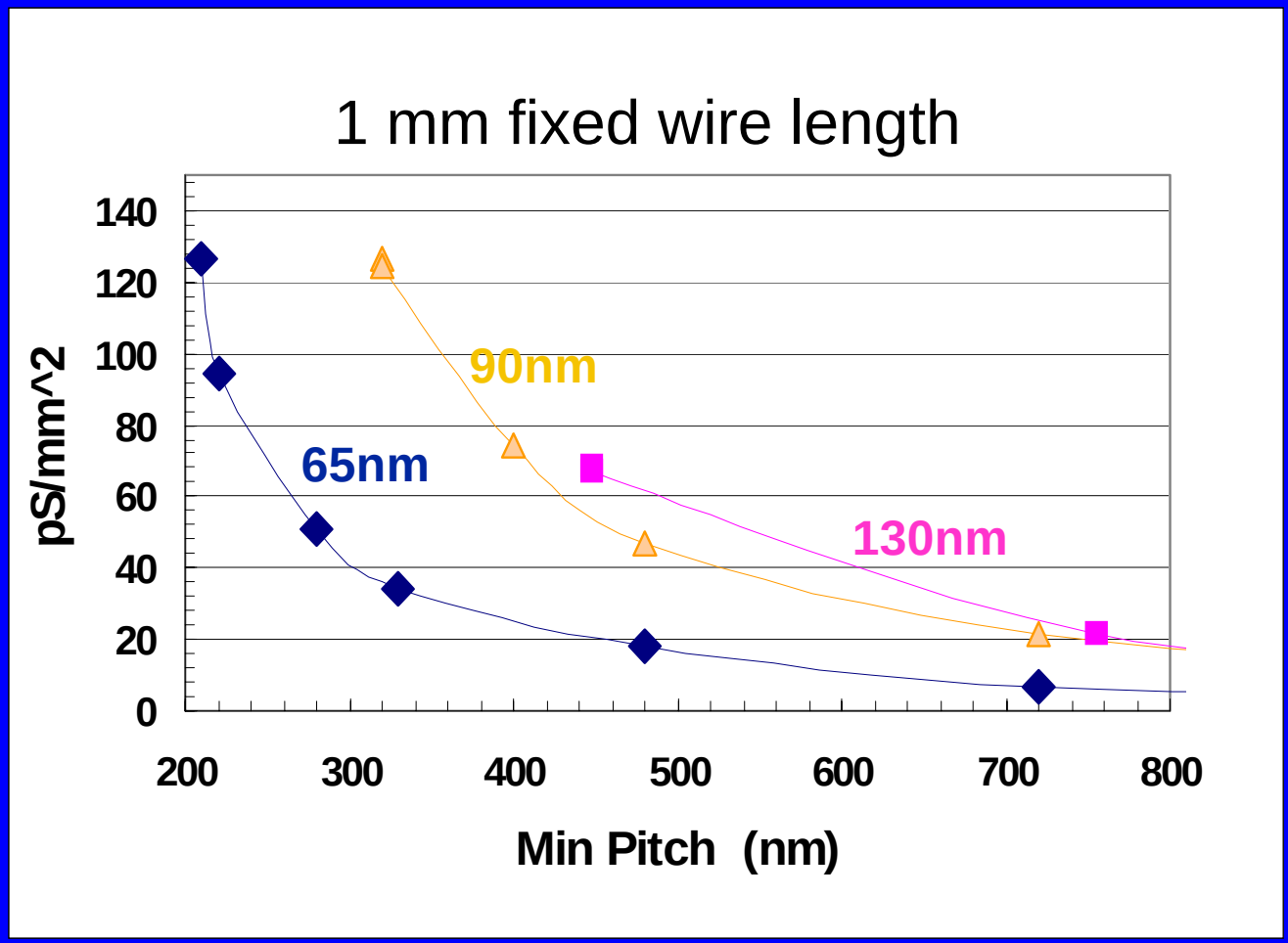
NiSi gate resistance well controlled down to 30 nm L_G

8 Layers Cu Interconnect

- Dual damascene Cu
- 1.8 T/W aspect ratio
- CDO low-k ILD
- SiCN etch-stop layer replaces SiN for 5% total ILD cap reduction
- Graduated pitches for optimizing density vs. performance

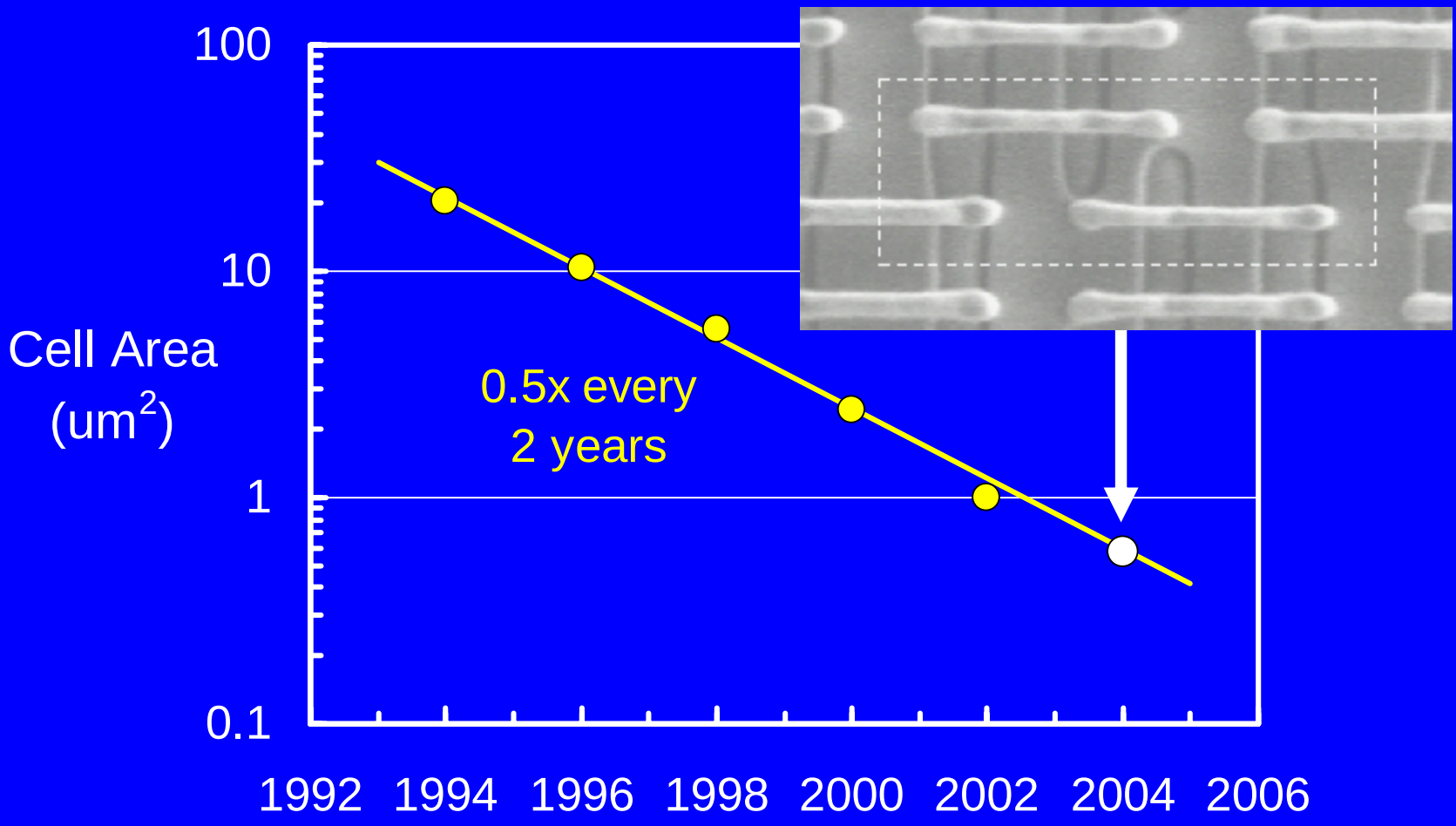


Interconnect RC Performance



65 nm continues the intrinsic RC improvement

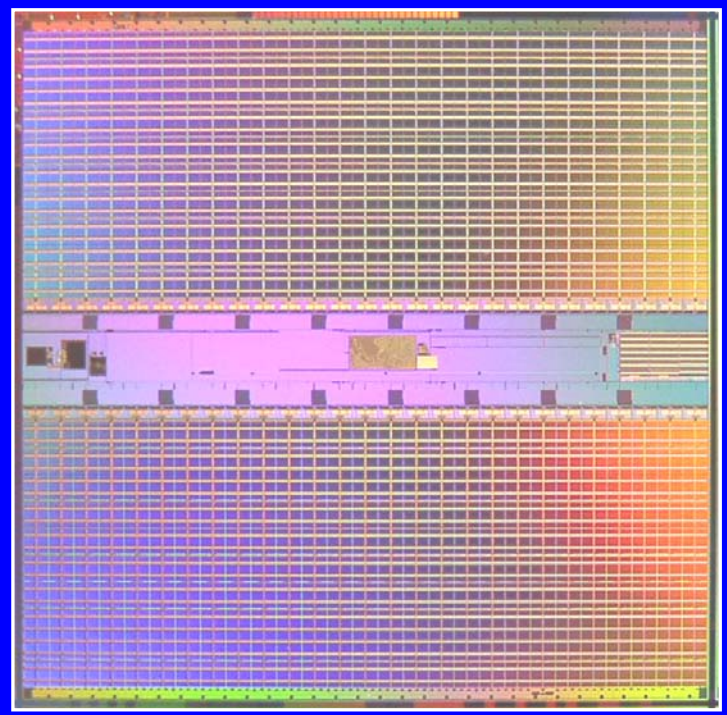
0.57 μm² 6-T SRAM Cell



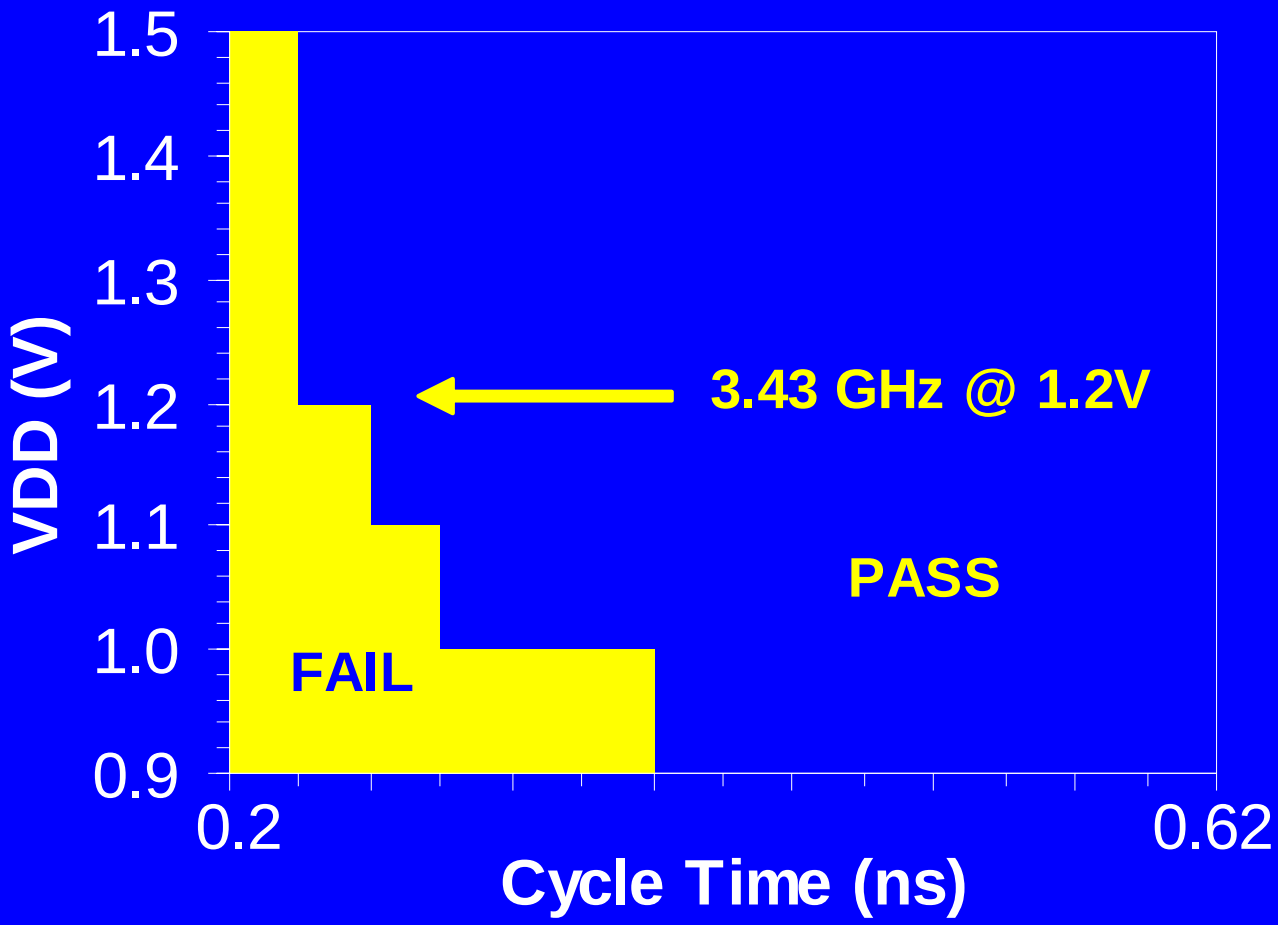
Transistor density continues to double every 2 years

High Performance 70 Mbit SRAM

- 0.57 μm^2 cell size
- >0.5 billion transistors
- 110 mm^2 chip size
- Uses all process features
- Capable of supporting Vdd at 0.7V.
- Fully functional 70 Mbit SRAM chips have been fabricated.

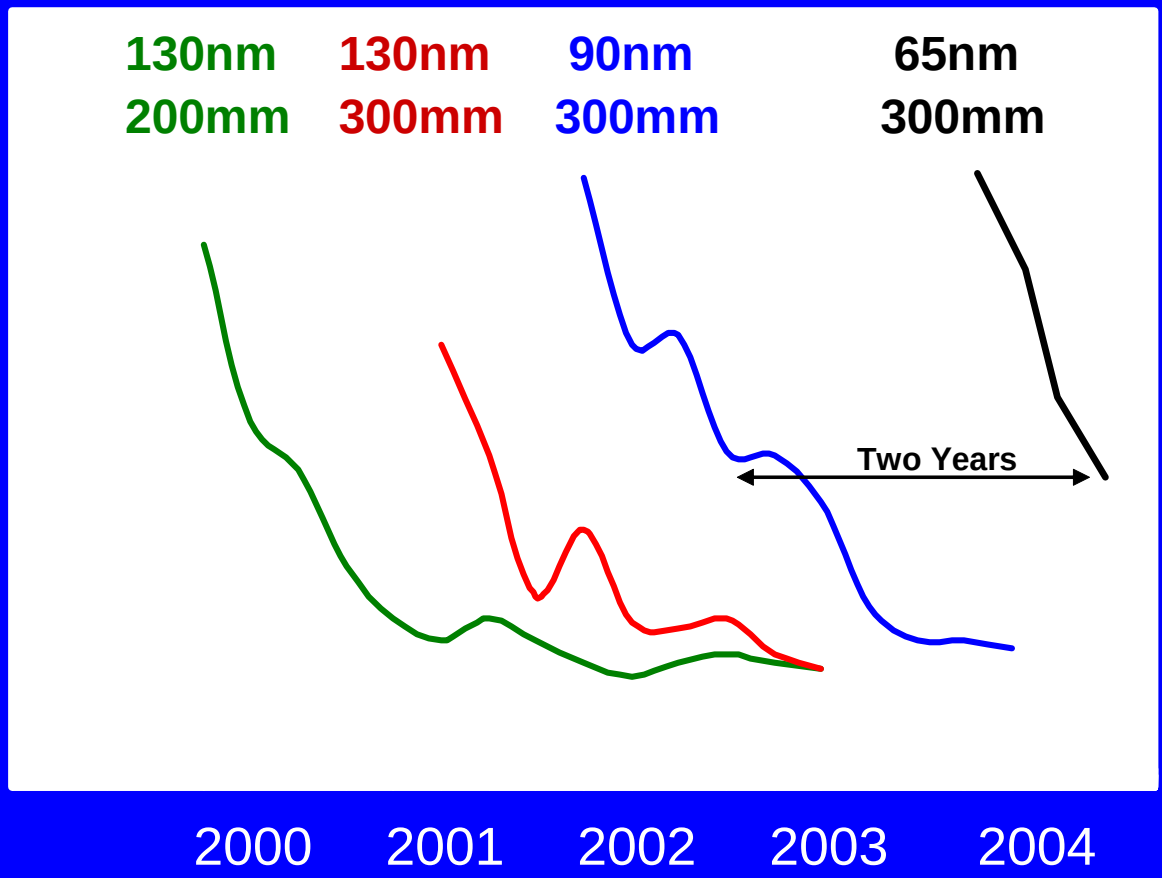


High Performance 70 Mbit SRAM



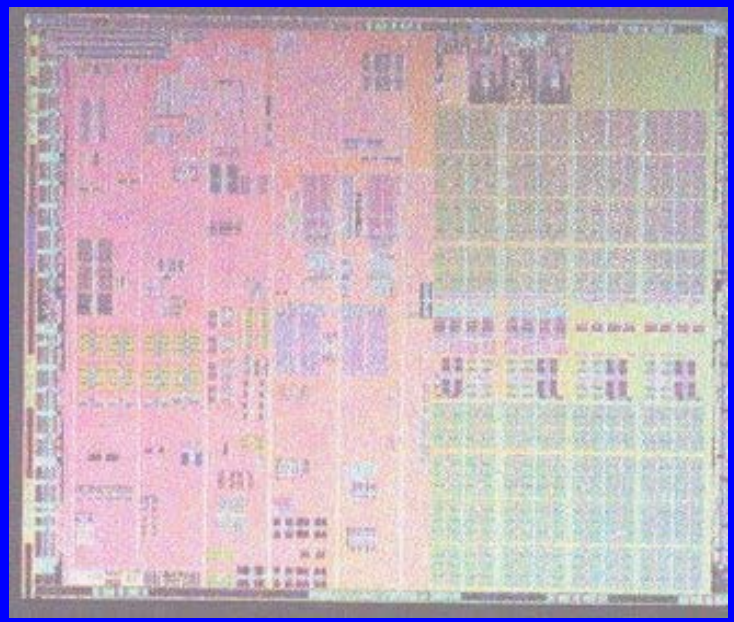
Demonstrated 3.43 GHz at 1.2V

Defect Reduction Trend

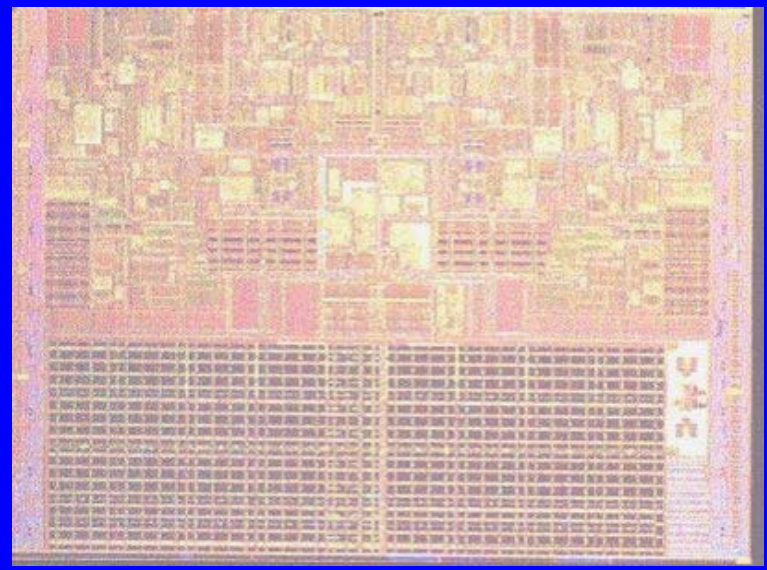


65 nm yield on same improvement rate with 2 years offset

65 nm Microprocessor Prototypes Fabricated



Single Core



Dual Core

65 nm process ready for high volume manufacturing in 2005

Conclusion

- An industry leading 65 nm logic technology is presented.
- Continues Moore's law, with the same density improvement rate as previous generations.
- Record transistor drive currents achieved by Intel's unique strained silicon technology.
- Cu and low-k ILD interconnect with superior RC performance.
- Excellent yield demonstrated on 70 Mb SRAM, with 0.57 μm^2 SRAM cell size and low voltage operation.
- Microprocessor prototypes have been fabricated. The process will be ready for high volume manufacturing in 2005, two years after the 90nm technology.

Acknowledgments

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  - Portland Technology Development
  - Sort Test Technology Development
  - Quality and Reliability Engineering
  - Technology Computer Aided Design

For further information on Intel's silicon technology, please visit the Silicon Showcase at

www.intel.com/research/silicon